

[METHOD FOR FETCHING WORD INSTRUCTION IN A WORD-BASED PROCESSOR AND CIRCUIT TO PERFORM THE SAME]

Abstract of Disclosure

The invention is directed to a method for fetching at least one word instruction in a word-based processor. The word instruction includes several types of a full-word instruction or a half-word instruction. The processor employs a data bus with a word length in bit. The method includes dividing the word length into a plurality of word units by 2^n bits. The processor checks the memory request to obtain whether or not the word instruction to be fetched is in a sequential half-word aligned address. If it is, then the processor fetches the sequential multiple half-word instructions at the same time in full word length at a first fetch cycle. The half-word instructions are stored in the word units. Then, the half-word instructions are executed without directly fetching the half-word instructions from the memory in each the fetch cycles. A circuit is also provided to fetch the word instruction.

Figures

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